MATERIALS FOR THIN FILM TRANSISTORS FABRICATION AT LOW TEMPERATURE

Carlos Eduardo Viana [1]
Otávio Filipe da Rocha [2]
João Vicente Zampieron [3]
Luiz Carlos Donizetti Gonçalves [4]
Nilton Itiro Morimoto [5]

Abstract

In this work we present and discuss about the different kinds of materials to fabricate thin film transistors – TFTs - in low temperature process regime. The materials used in this work are: aluminum, amorphous silicon, silicon oxide and palladium. Main focus of this work is the insulator silicon oxide deposition process – PECVD. The results presented are: deposition rate as a function of substrate temperature curve, FTIRS spectra and obtained electric properties by implemented MOS capacitors (aluminum / silicon oxide / monosilicon substrate), i.e. flat-band voltage, dielectric constant, effective charge density, leakage current at 5 MV/cm and breakdown strength. Finally the perspectives and next steps of the process to fabricate thin films transistors at low temperature are presented.

Key-words: PECVD-Tetraethylorthosilicate; Low temperature deposition silicon oxide; Thin film transistors.

60° Congresso Anual da Associação Brasileira de Materiais, Belo Horizonte/MG, 25 a 28 de Julho de 2005 (Materiais compósitos, poliméricos, elétricos e magnéticos)

[1] *Associated Researcher at EPUSP – PhD in Microelectronics at EPUSP;*

[2] *Microelectronics Master Student at EPUSP;*

[3] *Universidade Sant'Anna - Depto. Engenharia de Computação – PhD in Nuclear Technology - Materials at INPE;*

[4] *Associated Researcher at EPUSP – PhD in Physics at IFUSP;*

[5] *Staff of Universidade de São Paulo -PhD in Microelectronics at EPUSP.*

LSI - Laboratório de Sistemas Integráveis - EPUSP – Escola Politécnica da Universidade de São Paulo – Brazil - Av. Professor Luciano

INTRODUCTION

Amorphous and polycrystalline silicon thin-film transistors – TFTs - have been extensively investigated for applications in large-area electronics, especially for active matrix liquid crystal displays (AMLCDs) **[1-4]**. The required process temperature to realize these applications was about 600°C.

Nowadays, TFTs fabricated with low temperature process (from 150-300°C) **[5,6]** and also with room temperature **[7,8]** and over glass or plastic subtracts have attracted much attention. The widespread application of TFTs over plastic substrates is expected because of the low temperature process and low cost [**9**].

In this work we discuss the materials properties to be deposited in glass and/or plastic substrates, it means very low process temperature **[10]**. These materials are: palladium as bottom contact, silicon oxide as gate dielectric, amorphous silicon as active layer and aluminum as top contact.

Experimental results concerning on the above-mentioned thin films materials compatible with the process temperature supported by the subtracts were presented. Discussions about the next steps of the work are presented too.

EXPERIMENTAL

To deposit the silicon oxide layers it was used a home made PECVD – Plasma Enhanced Chemical Vapor Deposition - cluster tool system, as described before **[11]**. It has three process chambers, a load lock and a sample manipulation chamber.

Silicon wafers (100), p-type, 7-13 Ω.cm, 75 mm in diameter were used as test samples substrates. These substrates were cleaned using the piranha (4:1 H_2SO_4:H_2O_2) and RCA standard cleaning processes followed by a dip in diluted HF.

Silicon oxides depositions were carried out using the process parameters presented in Table 1. TEOS and oxygen are mixed in a special chamber before entering the process reactor to guarantee a homogeneous gas mixture.

Deposition processes were started with O_2 plasma using the conditions showed in Table 1. After 30 s, TEOS was inserted into reactor. This procedure was used to prevent the contact of un-cracked TEOS with the substrate, which minimize the incorporation of its sub-products into the silicon-oxide interface. After deposition, the TEOS flow was closed and pure O_2 plasma was maintained during one minute. This procedure was performed to minimize the formation of dangling bonds on the oxide surface and to promote the reaction of any TEOS sub-products adsorbed on the deposited film **[12]**. Prior to deposition process, a plasma cleaning procedure, based on a mixture of CF_4 and O_2, was performed to ensure the same initial deposition conditions.

Monitor samples were deposited in order to obtain accurate measurements of refractive index, about 1.39 at 632.8 nm, which suggests low-density silicon oxides **[12]**. Film thickness of capacitor samples was then measured by ellipsometry. Fourier Transform Infrared Spectroscopy (FTIRS) was used to determine the chemical bonding states. Electrical characterization of silicon oxide films (about 50 nm thick) was performed using MOS capacitors with 1.08×10^{-3} cm^2 of area. Aluminum films, 300 nm thick, were evaporated at a pressure of 5×10^{-6} mbar. These

capacitors were characterized by JE (current density versus breakdown strength) and HF-CV (high frequency capacitance versus voltage at 1 MHz) measurements, carried out in an automatic Hewlet Packard test station.

Table 1. Silicon oxide deposition process parameters for all PECVD-TEOS samples.

Pressure, **P**	1 Torr
Distance between electrodes, **d**	15 mm
RF Power, $\mathbf{W_{RF}}$	400 W
Oxygen Flow, $\mathbf{F_{O2}}$	200 sccm
TEOS Flow, $\mathbf{F_{TEOS}}$	2 sccm
Substrate Temperature, **T**	$25^{\xi} \leq T \leq 375°C$

$^{\xi}$ In the process at room temperature, the substrate temperature reached up to 150°C due only the plasma bombardment during the process.

Monitor samples were deposited in order to obtain accurate measurements of refractive index, about 1.39 at 632.8 nm, which suggests low-density silicon oxides **[12]**. Film thickness of capacitor samples was then measured by ellipsometry. Fourier Transform Infrared Spectroscopy (FTIRS) was used to determine the chemical bonding states. Electrical characterization of silicon oxide films (about 50 nm thick) was performed using MOS capacitors with 1.08×10^{-3} cm^2 of area. Aluminum films, 300 nm thick, were evaporated at a pressure of 5×10^{-6} mbar. These capacitors were characterized by JE (current density versus breakdown strength) and HF-CV (high frequency capacitance versus voltage at 1 MHz) measurements, carried out in an automatic Hewlet Packard test station.

Palladium films are deposited by joule effect in an evaporator system under a pressure of 5×10^{-6} mbar and at room temperature.

Amorphous silicon films with 1 nm of thickness are deposited by a sputtering system at room temperature and under a pressure of 1×10^{-7} Torr with a 99.9999 pure silicon target in argon plasma.

RESULTS AND DISCUSSIONS

Silicon Oxide

Higher deposition rates were attained for lower process temperatures (**Figure 1 a**). This effect was assigned in previous works to a possible incorporation of organic TEOS sub-products **[6,8,13]**. These TEOS films deposited at low temperatures formed a gel-like and porous structure. However, for our samples, carbon compounds signals were not detected in FTIRS, within the sensitivity of these measurements. We are led; therefore, to believe that low temperatures did not promote an efficient migration of plasma generated species on samples' surface. A lower compactation degree is expected since deposition rate is higher than the time for such species to find lower energy active sites, and also such samples obtained at lower temperatures shall present a high concentration of oxide charge. For temperatures above 225°C, therefore, lower deposition rates indicate more compact films with a smaller charge density (see Table 2).

Figure 1 b) presents the FTIRS spectra of the deposited SiO_x for the different

deposition temperatures. Samples exhibit the Si–OH related absorbance peaks between 930 and 940 cm^{-1}. For lower deposition temperatures, this peak is more pronounced, since less dense oxides films are expected, and therefore more hygroscopic. Si-OH peak weakens as the process temperature is increased. Deshmuch et al. reported this effect for TEOS-SiO_x samples obtained from room temperature up to 250°C. These authors also pointed out that low deposition rates and low partial pressure of TEOS lead to good quality SiO_x films **[8,14]**. The dissociation of TEOS sub products is improved for more energetic processes. The content of Si-OH bonds is also a measurement of space filling: higher contents of these bonds indicate less dense, hydrophilic films **[15]**. Additionally, the Si-O stretching peak, between 1.070 and 1.085 cm^{-1}, shifts towards lower wavenumbers as deposition temperature increases (**Figure 1 b**), suggesting an increase in film's density **[12]** or strain **[16]**.

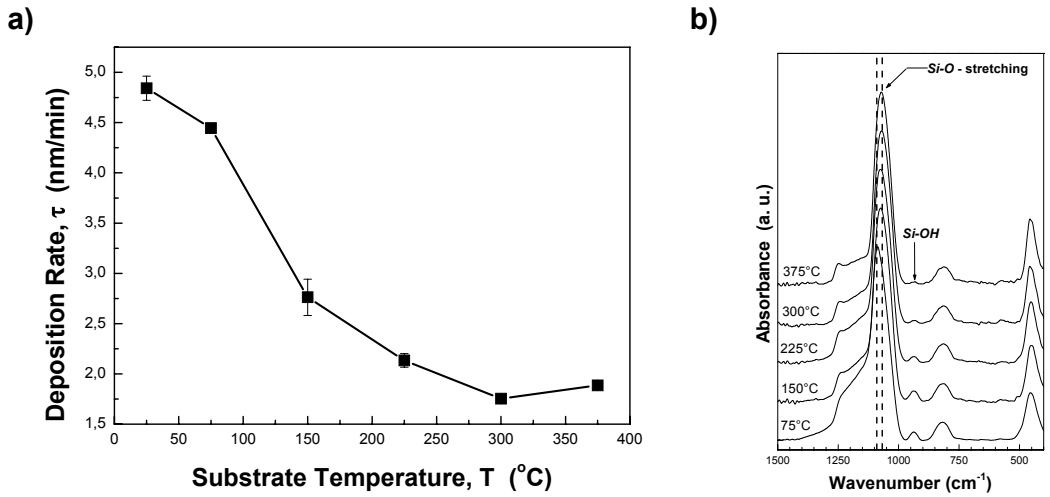

Figure 1. a) Deposition rate as a function op substrate temperature, where higher deposition rates are obtained for lower process temperatures, attributed to the possible incorporation of non-dissociated TEOS sub products. **b)** FTIRS spectra as a function of the substrate temperature. For lower temperatures, the Si-OH peak intensity increases, indicating a more hygroscopic character to the deposited films.

Table 2 summarizes the electrical characteristics of films according to deposition temperature. The best results were those for the samples deposited at higher temperature. The samples deposited at 225°C presented some capacitors with ε_{ox} = 3.9 and E_{BD} = 11.85 MV/cm. 225°C can be considered as the lower bound of temperature to obtain films with similar electric properties.

Higher dielectric constants were obtained for samples deposited at lower temperatures due to the post deposition water incorporation.

The higher charge densities were obtained for the films deposited at lower temperatures due to their more defective structure.

Table 2. Sample parameters obtained from HF-CV and JE measurements of MOS capacitors: flat-band voltage (V_{FB}), dielectric constant (ε_{ox}), effective charge density (Q_{SS}/q), leakage current at 5 MV/cm (J_{LK}) and breakdown strength (E_{BD}).

Substrate Temperature	V_{FB} (V)	ε_{ox}	Q_{SS}/q (cm^{-2})	J_{LK} (A/cm^2) at 5 $MV.cm^{-1}$	E_{BD} ($MV.cm^{-1}$)
[ξ] 25ºC	-2.25	8.49	$1.39x10^{12}$	> >	2.98
150ºC	1.66	4.73	$1.30x10^{12}$	$1.47x10^{-6}$	9.68
225ºC	4.61	4.17	$1.99x10^{12}$	$6.69x10^{-7}$	10.24
300ºC	0.73	3.84	$6.17x10^{11}$	$4.70x10^{-7}$	9.46
375ºC	-0.78	4.14	$9.97x10^{10}$	$7.60x10^{-7}$	8.51

[ξ] In the process at room temperature, the substrate temperature reached up to 150°C due only the plasma bombardment during the process.

Palladium, Aluminum and Silicon Thin Films Obtention

Palladium (500 nm tick) and aluminum (300 nm tick) films are deposited by Joule effect in an evaporator deposition system. The films deposited were uniform in thickness and very reproductible, and these films were extensively studied **[17]**.

To perform the TFTs it is necessary to wet etch the aluminum film. This step must be compatible with the palladium film and not change it properties. To etch the aluminum film it was used the solution presented in **Equation 1** and the etch rate after the aluminum oxide etch is approximately 200 nm/min under 40°C.

Equation 1: $35\ H_3PO_4 + 3\ HNO_3 + 14\ H_2O$ @ 40°C

Palladium films were not attached by the **Equation 1** solution showing the viability to be employed as a step of all the process to fabricate the TFTs at low temperature.

Amorphous silicon films with 1 nm of thickness are deposited by a sputtering system at room temperature and under 5 x 10^{-7} Torr with a 99.9999 pure silicon target.

A plasma wet etch reactor chamber was used to pattern both silicon and silicon oxide with a gas mixture of O_2 and SF_6, the etch rate was 150 nm/min at 50 W of RF applied power.

TFTs Process

Figure 2 shows the thin film transistor cross sectional view that will be fabricated in low temperature process and with the discussed materials in this work, i.e. aluminum, amorphous silicon, silicon oxide and palladium.

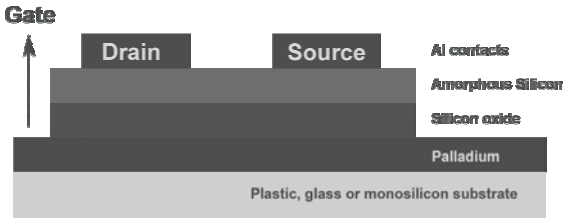

Figure 2. Cross sectional view of TFT proposed to be fabricated: First, a palladium film is deposited to make the bottom contacts followed by silicon oxide deposition to gate insulator and amorphous silicon as active layer of the transistor. Patterning of mask 1 is performed to define both silicon and oxide films. After that, an aluminum film to drain and source contacts is deposited and finally, mask 2 is patterned to define the aluminum contacts. All steps are carried up at temperatures lower than 150°C.

PERSPECTIVES

Obtention processes to different materials are discussed in this work aiming the TFTs fabrication in low temperature.

Silicon oxide films deposited by PECVD were characterized and its properties were also presented. These films are suitable to be employed as gate dielectric in TFTs.

Metal contacts like Pd and Al were characterized concerning on its applications and restrictions to be employed in the TFTs process.

Amorphous silicon was also obtained and the wet etch rate was obtained.

Finally all the materials films are already obtained and characterized. Next step is to realize the thin films transistors as presented at the **Figure 2**.

Acknowledgements

The authors would like to thank J. A. R. Porto, who provided the technical support. The financial support from Millennium Institute and PDI&TI CNPq programs are gratefully acknowledged.

BIBLIOGRAPHY

[1] C. T. Angelis, C. A. Dimitriadis, M. Myasaka, F. V. Farmakis, G. Kamarinos, J. Brini, J. Stoemenos, Effect of excimer laser annealing on the structural and electrical properties of polycrystalline silicon thin-film transistors, J. Appl. Phys. v.86 (8), p.4600-4606, 1999.

[2] R. Dassow, J. R. Kohler, Y. Helen, K. Mourgues, O. Bonnaud, T. Mohammed-Brahim and J. H. Werner, **Laser crystallization of silicon for high-performance thin-film transistors**. Semicond. Sci. Technol. v.15 (2000) L31–L34, 2000.

[3] K. Mourgues, F. Raoult, T. Mohammed-Brahim, D. Briand, O. Bonnaud, **Performance of thin film transistors on unhydrogenated in-situ doped polysilicon films obtained by solid phase crystallization**, Mat. Res. Soc. Symp. Proc., v. 471, 1997, p.155-160.

[4] K. J. Nieuwesteeg, A. H. van Ommen, "**AM-LCDs bring solid-state devices to the display**. Proceedings of the 27th European Solid-State Device Research Conference, ESSDERC'97, Stuttgart, Germany, v.22-24 Sept, p.88-100, 1997.

[5] Dong S. Kim, Young H. Lee, **Room-temperature deposition of a-SiC:H thin films by ion-assisted plasma-enhanced CVD**. Thin Solid Films, 1996, v.283, p.109-119, 1996.

[6] Nur Selamoglu, John A. Mucha, Dale E. Ibbotson, and Daniel L. Flamm, **Silicon oxide deposition from tetraethoxysilane in a radio frequency downstream reactor: Mechanisms and step coverage**. J. Vac. Sci. Technol. B, 1989, v.7, i.6, 1345-1351. 1989.

[7] Young-Bae Park, Jin-Kyu Kang and Shi-Woo Rhee, **Effect of N_2O/SiH_4 ratio on the properties of low-temperature silicon oxide films from remote plasma chemical vapour deposition**. Thin Solid Films, v.280, Iss.1-2, p.43-50, July 1996.

[8] Shashank C. Deshmukh and Eray S. Aydil, **Investigation of SiO_2 plasma enhanced chemical vapor deposition through tetraethoxysilane using attenuated total reflection Fourier transform infrared spectroscopy**. J. Vac. Sci. Technol. A, 1995, v.13, p.2355-2367, 1995.

[9] Y. Fujisaki, Y. Inoue, T. Kurita, S. Tokito, H. Fujikake and H. Kikuchi, **Improvement of Characteristics of Organic Thin-Film Transistor with Anodized Gate Insulator by an Electrolyte Solution and Low-Voltage Driving of Liquid Crystal by Organic Thin-Film Transistors**. Jpn. J. Appl. Phys, v.43, n.1, 2004, p.372-377. 2004.

[10] D. Briand, M. Sarret, P. Duverneuil, T. Mohammed Brahim and K. Kis Sion, **Influence of the doping gas on the axial uniformity of the growth rate and the electrical properties of LPCVD in situ doped polysilicon layers**, J. Phys. IV, v. 5, p.887, 1995.

[11] N. I. Morimoto, J. W. Swart, **Development of a Cluster Tool and Analysis of Deposition of Silicon oxide by TEOS/O_2 PECVD**. Rapid Thermal and Integrated Processing V, Mat. Res. Soc. Symp. Proceedings, v.429, 1996, p.263-268.

[12] L. C. D. Gonçalves, C. E. Viana, J. C. Santos, N. I. Morimoto; **Correlation between mechanical and electrical properties of silicon oxide deposited by PECVD-TEOS at low temperature**. Surface & Coatings Technology, v.180-181C, p.275-279; 2004.

[13] K. Aumaille, C. Vallée, A. Granier, A. Goullet, F. Gabouriau, G. Turban, **A comparative study of oxygen/organosilicon plasmas and thin $SiO_xC_yH_z$ films deposited in a helicon reactor**. Thin Solid Films, v.359, Iss.2, 31 January 2000, p.188-196.

[14] Sang M. Han and Eray S. Aydil, **Study of surface reactions during plasma enhanced chemical vapor deposition of SiO[sub 2] from SiH[sub 4], O[sub 2], and Ar plasma**. J. Vac. Sci. Technol. A, v.14, Iss.4, p.2062, 1996.

[15] N. Hirashita, S. Tokitoh, H. Uchida, **Thermal Desorption and Infrared Studies of Plasma-Enhanced Chemical Vapor Deposited SiO Films with Tetraethylorthosilicate**. Jpn. J. Appl. Phys., v.32, n.4, p.1787-1793, 15 April 1993.

[16] J. T. Fitch, C. H. Bjorkman, G. Lucovsky, F. H. Pollak, X. Yin; **Intrinsic stress and stress gradients at the SiO[sub 2]/Si interface in structures prepared by thermal oxidation of Si and subjected to rapid thermal annealing**. J. Vac. Sci. Technol. B, v.7, Iss.4, p.775-781 1989.

[17] J. V. Zampieron, L. S. Zambom, N. I. Morimoto, **Study of metallic thin films of palladium using evaporation technique**, Proceedings on Workshop on Semiconductors and Micro & Nano-Technology – SEMINATEC 2005. Auditorium of Central Library, UNICAMP, Campinas/SP, March 4th, 2005.

MATERIAIS PARA A FABRICAÇÃO DE TRANSISTORES DE FILMES FINOS A BAIXA TEMPERATURA

Carlos Eduardo Viana [1]
Otávio Filipe da Rocha [2]
João Vicente Zampieron [3]
Luiz Carlos Donizetti Gonçalves [4]
Nilton Itiro Morimoto [5]

Resumo

Neste trabalho são apresentados e discutidos diferentes tipos de materiais para fabricação de transistores de filmes finos – TFTs – utilizando baixa temperatura de processamento. Os materiais utilizados neste trabalho são: alumínio, silício amorfo, óxido de silício e paládio. O foco principal deste trabalho é o processo de deposição de filmes de óxido de silício – PECVD. Os principais resultados apresentados são: taxa de deposição em função da temperatura do substrato, espectros FTIRS e suas propriedades elétricas através da implementação de capacitores MOS (alumínio / óxido de silício / substrato de silício monocristalino), ou seja: tensão de banda-plana, constante dialética, densidade efetiva de cargas, corrente de fuga a 5 MV/cm e campo elétrico de ruptura da rigidez dialética. Finalmente as perspectivas e próximas etapas do processo de fabricação dos transistores de filmes finos a baixa temperatura de processamento são apresentadas.

Palavras-chave: Etraetilortosilicato - deposição química a vapor enriquecida por plasma; Deposição de [óxido de silício a baixa temperatura; Transistores de filmes finos.

60° Congresso Anual da Associação Brasileira de Materiais, Belo Horizonte/MG, 25 a 28 de Julho de 2005 (Materiais compósitos, poliméricos, elétricos e magnéticos)

[1] *Associated Researcher at EPUSP – PhD in Microelectronics at EPUSP;*

[2] *Microelectronics Master Student at EPUSP;*

[3] *Universidade Sant'Anna - Depto. Engenharia de Computação – PhD in Nuclear Technology - Materials at INPE;*

[4] *Associated Researcher at EPUSP – PhD in Physics at IFUSP;*

[5] *Staff of Universidade de São Paulo -PhD in Microelectronics at EPUSP.*

LSI - Laboratório de Sistemas Integráveis - EPUSP – Escola Politécnica da Universidade de São Paulo – Brazil - Av. Professor Luciano